120 MHz, 2.2 mW Low Power Phase-Locked Loop using Dual Mode Logic and its Application as Frequency Divider

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Abstract: Phase Locked Loop (PLL) frequency synthesizers are widely used in all forms of radio communications equipment today. It is used for generating a user selectable set of frequencies from a single reference. In this paper, conventional PLL using CMOS logic (Complementary Metal Oxide Semiconductor) and DML logic (Dual Mode Logic) are used to design the PLL to obtain a frequency of 120 MHz The internal transistor level involves CMOS logic and dual mode logic. Designed circuit is simulated using SPICE at transistor level 45nm technology. A clock of 120MHz is generated from the 250 kHz reference signal. An application of the Dual mode PLL is used in the frequency divider circuit. The frequency divider is used to create a frequency of almost 800MHz.

Keywords: clock, counter, CMOS, frequency divider, loop filter, PLL

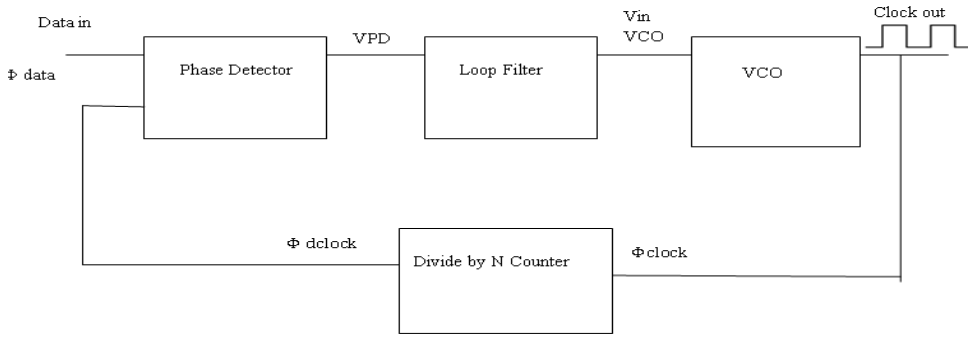
1. INTRODUCTION

The Phase Locked Loop (PLL) is one of the tools in the field of communication, and it is a feedback system that compares output frequency with the input frequency to attain the phase lock. Because of its wide variety of application such as frequency synthesizers, tracking satellite, demodulation, and telecommunication, it needs to operate with low power. They are used to retrieve the clock signal of the transmitted signal at the receiver end, by providing data synchronization at either side of communication circuits.

Phase-locked loop (PLL) is an important component in the transceiver. The disputes of mm-wave PLL design are high frequency, wide locking range, low phase noise, and low power [14]. However, generally there are trade-offs between these performances in CMOS technology [15]. The PLL requirements for automotive radars are demanding especially for the phase noise, because the close-in phase noise is a parameter of very strong influence to the resolution and sensitivity of a radar system. Many 24 or 77 GHz band CMOS PLLs have been reported, but their phase noise are limited by the classical PLL structure [16, 17]. This paper addresses the design of PLL using CMOS and Dual Mode logic and its performance analysis in terms of clock generation. An application of

PLL as frequency divider is taken into consideration.

The block diagram of a PLL is given in (Fig. 1). It consists of Phase Detector (PD), Loop filter, Voltage-Controlled Oscillator (VCO) and divide counter. The reference signal is 'data in'; which is either the received signal or the output of a local oscillator. The phases of the dynamically corrected clock and the reference signals are compared at the PD, which produces a high output signal in coincidence with the phase difference of the input



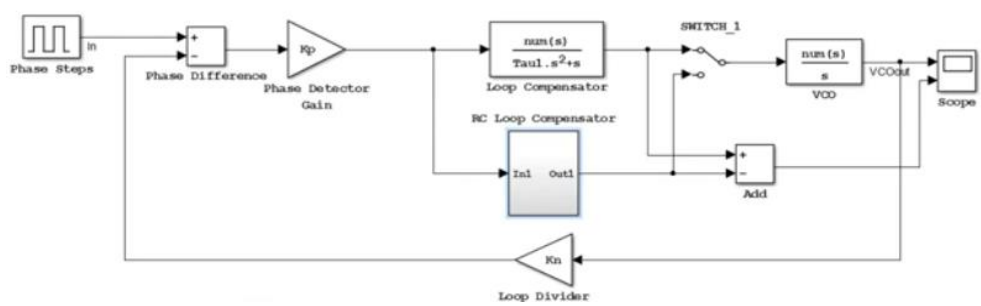
waveforms. The output signal from the PD is sent through the loop filter, a low pass filter that adds an extra pole to the circuit. To control the gain of the feedback loop the extra pole contributed by the VCO is essential; this prevents the lock of the output signal with a reference signal at higher order harmonics.

Fig. 1.Block Diagram of a PLL.

The Output of the VCO is the clock signal the converted form of phase information, whose frequency is controlled by the voltage of the PD after being processed by the loop filter. As the VCO output is fed back to the PD, the error has to be minimized by repeating the cycles which is N. This number N is set with the help of the counter that is to control the multiplication factor over the reference clock, to obtain locked output signal. The gains of the individual sub-block are used in the estimation of closed loop gain of PLL [1].

The overall closed loop gain becomes: $$H(s)=\frac{\Phi_{clock}}{\Phi_{data}}=\frac{K_{PD}K_{VCO}K_F}{s+\frac{1}{N}K_{PD}K_{VCO}K_F} \quad [1]$$

In the second order transfer function H(S), the S term is brought in by the VCO and filter. Theoretically, a first-order PLL [2], without a loop filter, can also work. However, as it



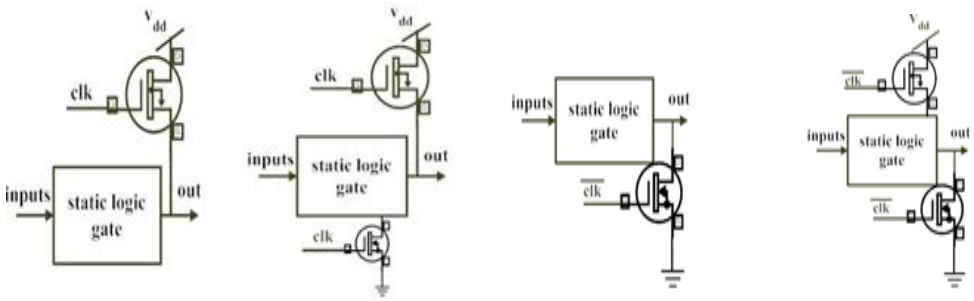
was pointed out [3], the second order system is simple to control and would permit

tracking of fast deviations in the time domain, thereby avoiding the system from locking onto higher order harmonics of the reference signal. (Fig. 2) represents the overall PLL design implemented in Matlab Simulink and tanner tool.

Fig. 2.Internal structure of a PLL in MATLab and Tanner EDA.

1.1Dual Mode Logic

Dual Mode Logic (DML) is used to combine the static and dynamic mode logic by utilizing the advantages of both modes. Static mode operates with low power consumption but with high delay, and the dynamic mode operates with high power consumption but with reduced delay. DML [4, 5] implementation uses an extra transistor in addition to the normal static gate, and the implementation is of two types. The extra transistor is linked with a global clock. In Type A realization as shown in Fig. 3(a), extra transistor



added is PMOS and is connected between the source and the output of the static gate. In Type, B implementation is shown in Fig. 3(b), additional transistor, NMOS that is connected between the ground and the output of the static gate. The extra transistor is used to provide the dynamic mode operation, and it avoids the need for an additional capacitor. DML is employed at the critical paths to reduce the delay and improve efficiency.

Fig. 3(a).DML Type A with Un-Footed and Footed Implementation.

Fig. 3(b).DML Type B with Un-Headed and Headed Implementation

1.2Phase Detector (PD) and Loop Filter

The illustration of the phase detector (PD) comprises of two D flip-flops and an efficient ‘AND' gate, that gives the feedback to their ‘CLR' pins. Equally the phase and the frequency of the inputs, A and B, affect the output of the PD. The two outputs of the PD are indicated, for reference purposes given as ‘upper’ and ‘lower' according to their position in the design. When ‘A’ is high than ‘B,' the upper output enters a high state following the first glance of the rising edge at input ‘A.' It would remain high in anticipation of another rising edge emerges at the input ‘B.' The changes in the ‘AND' gate and the high enabled ‘CLR' pins of the D flip- flops are caused by the transition in the lower output state to high. This high level at the ‘CLR’ pins resets the upper and lower outputs of the flip-flops. Then the output signals transmitted to the ‘CLR' pins through the ‘AND’ gate by creating a high to low transition, this is just like the PD is entering into a ‘watch’

mode. During the watch mode, both outputs are low, and the circuit thus waits for a rising edge of changing the state of either of the outputs.

To summarize, the upper output retains in high level among the successive rising edges of the inputs ‘A' and ‘B,' whereas the lower output has an instant peak for the duration of the rising edge of the input ‘B.' Same arguments hold fine when ‘B' leads ‘A,' except the roles of the upper and lower outputs are exchanged. PD of this category is capable of identifying the phase differences of $\pm 2\pi$, while it checks only at the rising edges of the input signal.

Next, to the block of PLL, PD is followed by a charge pump at the input of the loop filter. It is used to reduce the sensitivity of the charging and the discharging of the capacitors of the loop filter to the supply changes. The lower portion of the current sources is designed to supply a maximum of 70 μA , that is to drive the charge pump [19-22].

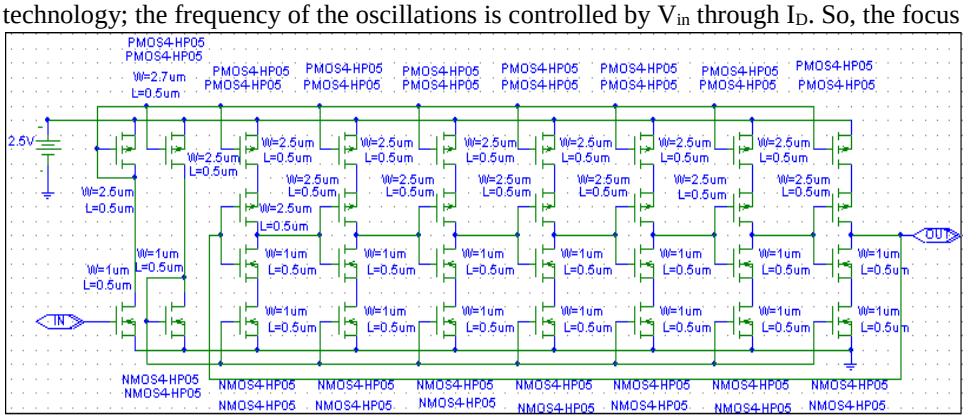
The loop filter is represented at the right-hand side of PD. If the upper output of the PD is high, i.e., the loop filter is represented at the right-hand side of PD. If the upper output of the PD is high, i.e., charging of the capacitor is done with the current source connected at the source of PMOS, when ‘A' is in logic 1 then ‘B, whereas the drain of the PMOS is coupled to the input of the filter. Similarly, when the lower output of the PD is high, i.e., ‘B' is higher than ‘A', the capacitor discharges through the source point of the NMOS. At the output side of PD, normally both outputs cannot go into a high state which is not in design reality. But they can be retained at low state thereby the collected charges are retained without any leakage through the 5kW resistor. The resistors are involved in leveling out output voltage when there are fast transients in the input signal.

1.3Voltage Controlled Oscillator (VCO)

The internal circuit schematic of the VCO is given in (Fig. 4). It is a current hungry ring oscillator. The frequency of oscillations of this circuit [2] is stated as follows:

$$f_{OSC} = \frac{I_D}{NC_{tot}VDD} \qquad [2]$$

Randomly, N is taken as 7 and VDD is kept at 2.5V. C_{tot} depends on the utilized technology; the frequency of the oscillations is controlled by V_{in} through I_D. So, the focus



is in designing symmetric current mirrors with linear current-voltage curves, which var-

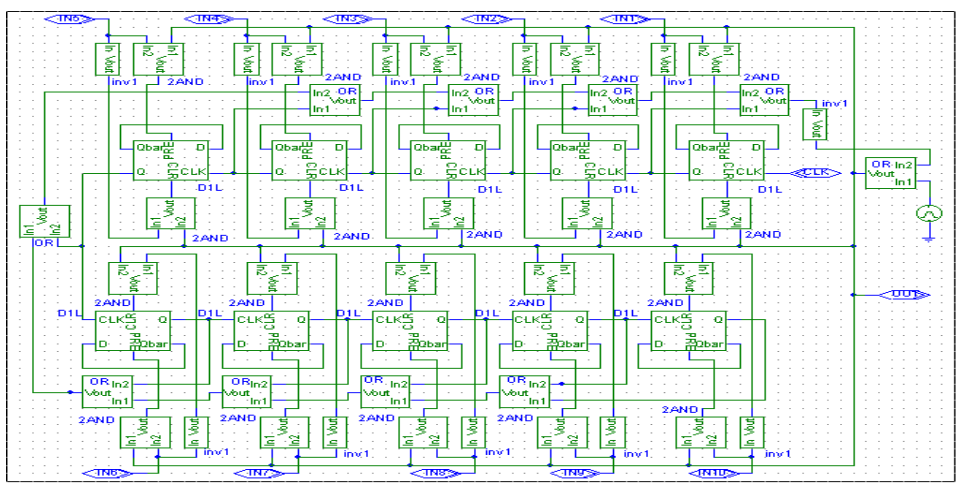
ies over the range of input voltages to give the oscillations around the operating range, which is between 100MHz and 250MHz for this design. The analysis shows that the boundaries of the operating range correspond to VCO input voltages of 0.9V and1.3V, respectively.

Fig. 4.The schematics of the VCO.

As a result, the aspect ratios of both current mirrors are tuned such that a symmetric linear I-V_{in} curve is achieved for the input voltages in the range of 0.9V-1.2V. The purpose of the adjusting the W/L ratios of the current mirrors involves in identifying few solutions of the system, since the relation of Vin-fosc focus on the quantity of the charges pumped through the mirrors [6,10,11]. But, the current mirrors are designed roughly at the initial stage, and then the input voltages are adjusted accordingly to identify the oscillations.

1.4Counter

The schematics of the designed 10-bit input, ripple carry type counter is shown in (Fig. 5). It is a down counter. Initial, setting or resetting each flip-flop depends on the input value at the D flip-flops. When the countdown starts; from the Q of each D flip-flop, the output is obtained. For this configuration, input D and the Qbar are tied together to trigger the change in Q value for each cycle. It continues until zero is reached,

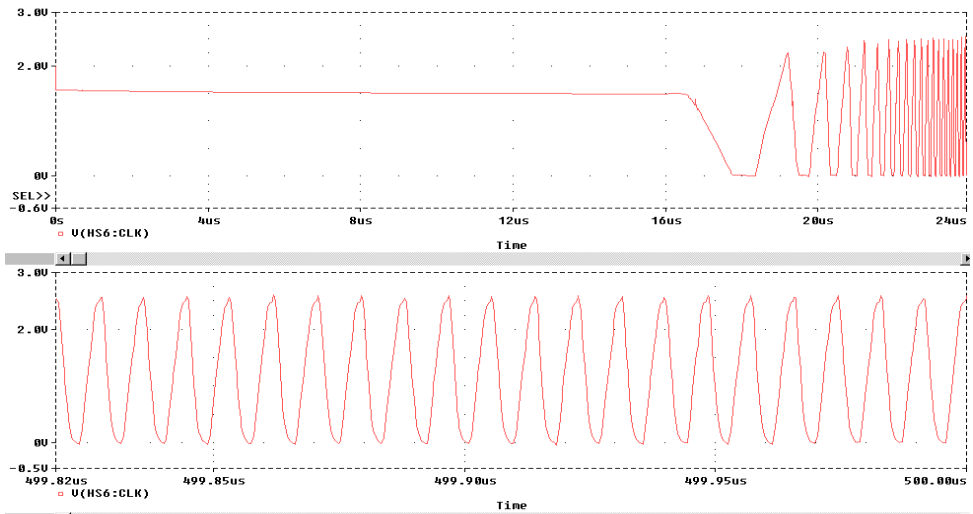


which is detected by the OR gates and ends in a resetting of the counter. In this proposed design a swallow counter [7, 12] and a 10-bit input counter was designed as the criterion was to achieve clock frequencies of 110 MHz to 130 MHz using the reference clock of 250kHz. It straightly converts to N values of 500 to 650. This decimal representation takes at least 10 bits to be given in binary. Swallow counter is used to prove the low power design and the required clock is obtained through the ripple counter.

Fig. 5. The Schematics of the 10-Bit Input Counter.

2. SIMULATION RESULTS

The internal sub-block of block diagram in (Fig. 6) is designed using the guidelines described before. The overall circuit is simulated using the previous designs with N set to



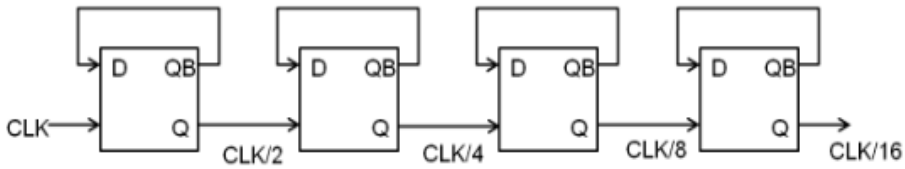
500 [8, 13] in the entire design the loop filter consisting of two capacitors which means it is a third order system. When the randomly chosen values are calculated from the equations, the natural frequency and the damping factor obtained as 125 kHz and 0.15, respectively. Although, the damping value founds to be much lower than the optimum value of 0.707, the importance of the design is for fast locking, other factors are not considered much.

Fig. 6.VCO Output at the Start and the End of the Simulation.

VCO output at the starting and the end of the simulation is shown in Figure.6. It is attractive to make a note of the output of the VCO which resides at a dc offset value until on 16μs, from the variation of input from 0.6v to 0.7v threshold value for the oscillations to initiate. After the iterations, the VCO output is inferred to have oscillations amid a frequency of 120MHz, for the number of cycles N=500.

3. APPLICATION OF DUAL MODE PLL DESIGN – FREQUENCY DESIGN

The targeted output clock frequency of the PLL in this paper is almost greater than 800MHz. In the case of the input reference clock frequency of 120MHz, a divide-by-16 frequency divider is required. The frequency divider consists of 4cascaded divide-by-2 stages as shown in (Fig. 7).



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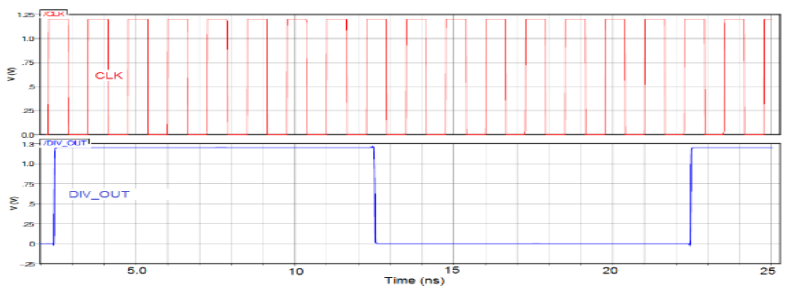


7.Divide by 2 circuits and transistor level diagram.

Though there is the possible architecture of divide-by-2 circuits, the D-flip-flop divider topology is the best suite for low power applications. The topology of divide-by-16 frequency divider is depicted in (Fig. 8).

Fig. 8. Divide by 16 arrangements.

The frequency divider is simulated for an input frequency of 800MHz is represented in (Fig. 9). The frequency divider shows a linear relationship between the input and output frequency with a slope of 1/16 for the input frequency up to 120MHz.

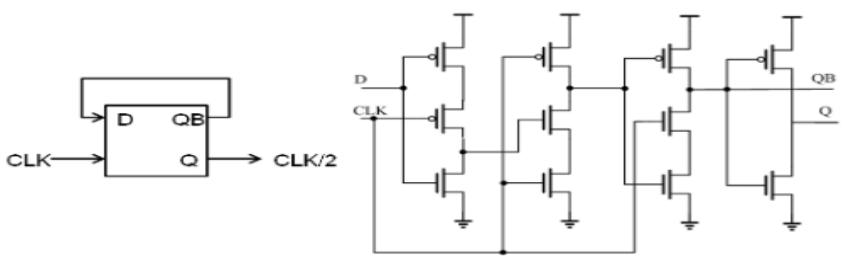
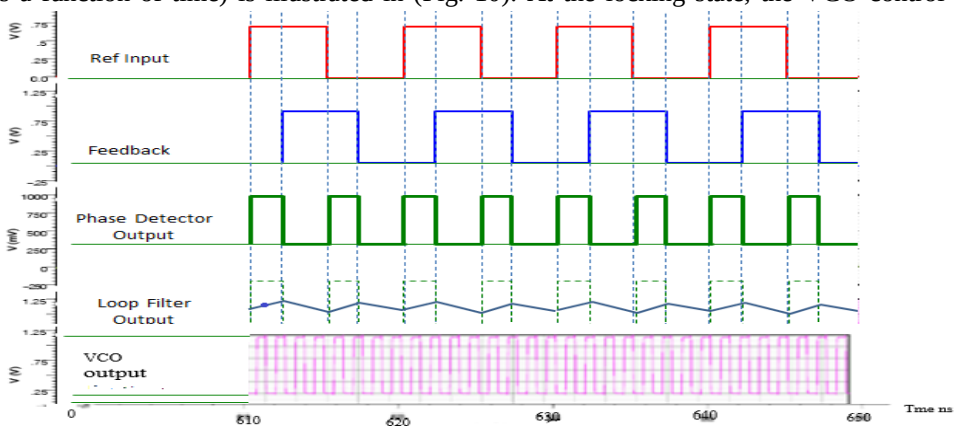


Fig. 9.

Frequency divider simulation with a reference frequency of 120MHz.

3.1PLL Locking Process

The PLL locking process in terms of VCO control voltage (VCO's control voltage as a function of time) is illustrated in (Fig. 10). At the locking state, the VCO control



voltage is 250mV, which is in the middle range between the ground and power supply. At the locking state, the PLL output frequency is stabilized at 800MHz, as design specifications required.

Fig. 10. PLL locking state for the frequency.

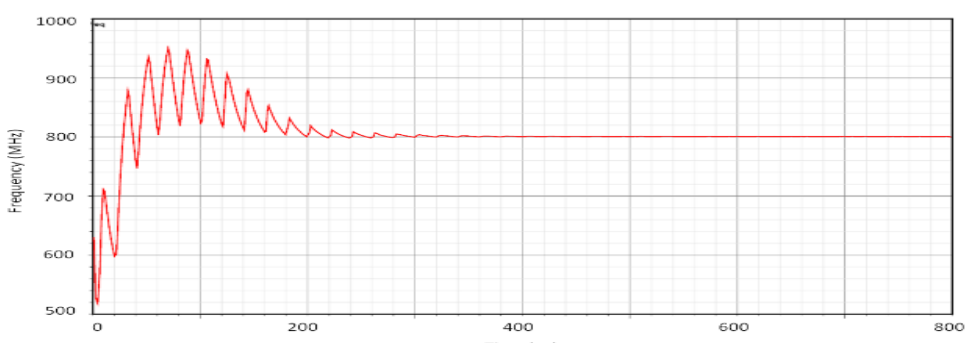
The simulations results indicate the estimated locking time is around 400ns. The reference signals (first), feedback signal (second), VCO signal (third) and PLL output signal (fourth) at the locking state are shown in (Fig. 11).

Fig. 11.Overall simulation output of the PLL and frequency divider circuit at the locking condition.

The reference signal (REF) and feedback signal (FB) is synchronized at the locking state with operation frequency of 120Hz. The VCO output has a voltage swing of 0.75 mV. One can also observe that the time for one period of the feedback signal is equal to 16 periods of PLL output clock, which indicates the frequency of the PLL output clock is 800MHz.

3.2Comparison of the PLL Design

Review of different techniques of PLL is addressed [8]; comparison of the proposed



work with the reference has been indicated in the Table 1.

Table 1 Power and Frequency Comparison of DML based PLL [8]

Technology - PLL	**Power Consumption**	**Frequency of operation**
High performance clock recovery circuit	18.6mW	3.2GHz
Current starved VCO	7.08mW	1.796GHz
OTA based ICO	0.34Mw	1GHz``
ADPLL	8mW	2.92GHz
QVCO	14.4mW	2.4GHz
Third order ,fully Integrated PLL	274mw	2GHz
Proposed DML based PLL	2.2mW	800MHz

It is found that though the technologies designed for PLL varies for different applications in terms of frequency, when considering power consumption, the proposed

PLL design with DML logic serves the best. As a frequency divider application of PLL it is capable to oscillate up to a frequency of 800MHz.

4. CONCLUSIONS

Considering the block by block design of PLL and its simulation in TSPICE with a technology file 45nm; it has been found that the initial design criterion is achieved by generating a clock signal at 120MHz using the reference signal of 250 kHz. The proposed design is compared with the swallow counter based PLL, but for low power, the dual mode logic holds good, for the frequency of oscillations the CMOS based ripple counter is efficient. Though there are glitches in the output waveforms, the design satisfies the constraint of generating clocks of required or optimum value. The peak power during the acquisition process is around 2.2mW, which is due to the VCO frequency overshoot. At locking state, the average PLL power consumption is 2mW with a certain range of fluctuation. The key cause for the instability is that transistors in VCO alternately go ON and OFF due to oscillation.

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